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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,358	01/27/2004	Toru Shimada	FUJZ 20.909	2902

26304 7590 08/08/2007

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EXAMINER	
ALI, FARHAD	

ART UNIT	PAPER NUMBER
2109	

MAIL DATE	DELIVERY MODE
08/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/766,358	SHIMADA, TORU	
	Examiner	Art Unit	
	Farhad Ali	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 1/29/2007
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by McFarland et al (US 5,226,126 A).

Claim 1

A data processing circuit comprising: a data processor which performs predetermined processing to data and outputs the data ([McFarland et al.] Column 3 Line 34 "CPU") having assigned thereto a processing destination identifier indicating a subsequent processing destination determined based on information included in the data ([McFarland et al.] Column 4 Line 11 "address preparation unit"); and a switch which provides the data to the subsequent processing destination based on the processing destination identifier ([McFarland et al.] Column 3 Line 48 "Instruction Decoder").

Claim 2

The data processing circuit as claimed in claim 1 wherein the predetermined processing comprises traffic processing ([McFarland et al.] Column 1 Line 57-58 "parallel processing of instructions within and between functional units").

Claim 3

The data processing circuit as claimed in claim 1, further comprising a line interface which provides the switch with the data having assigned thereto a processing destination identifier indicating the data processor which is a first processing destination ([McFarland et al.] Column 3 Lines 61-67 "DEC contains a fully associative Branch Prediction Cache" and "On each cycle, a macro-instruction is selected from one of the three instruction buffers or a branch target buffer in the BPC. The macro-instruction is decoded, assembled into an internal 96-bit decoded instruction word, referred to as a pseudo-op (p-op) or sometimes as an instruction or operation, and dispatched to the various functional units).

Claim 4

The data processing circuit as claimed in claim 1, further comprising a mother board which mounts the switch and a connector which connects the switch and the data processor ([McFarland et al.] Column 4 Lines 1-2 "Each functional unit chip is packaged in a custom ceramic PGA which contains power and ground planes"), and a controller which manages a configuration state of the data processor and notifies the configuration state to the data processor ([McFarland et al.] Column 4 Lines 1-2 "Each p-op issued by DEC 12 is given a tag which uniquely identifies each p-op currently outstanding in the machine" and Column 4 Lines 8-10 "DEC 12 is also responsible for tracking the status of outstanding p-op, pipeline control, and for invoking exception processing when needed").

Claim 5

The data processing circuit as claimed in claim 4, further comprising a memory which preliminarily stores the configuration state of the data processor provided to the controller ([McFarland et al.] Column 4 Lines 51-53 "DTag 32 contains the address tag and line state bits for each line in DCache 35").

Claim 6

The data processing circuit as claimed in claim 5, further comprising an input portion inputting the configuration state to the memory ([McFarland et al.] Column 4 Lines 30-33 "A Memory and Cache Controller (MCC) 25 is responsible for controlling the instruction and data caches and implements the cache coherency protocol").

Claim 7

The data processing circuit as claimed in claim 4 wherein the data processor has data processing identifier information indicating its data processing content, and the controller recognizes the configuration state by reading the data processing identifier information ([McFarland et al.] Column 4 Lines 1-2 "Each p-op issued by DEC 12 is given a tag which uniquely identifies each p-op currently outstanding in the machine" and Column 4 Lines 8-10 "DEC 12 is also responsible for tracking the status of outstanding p-op, pipeline control, and for invoking exception processing when needed").

Claim 8

The data processing circuit as claimed in claim 1 wherein the data processor has data processing identifier information which indicates its data processing content ([McFarland et al.] Column 4 Lines 1-2 "Each p-op issued by DEC 12 is given a tag which uniquely identifies each p-op currently outstanding in the machine"), and each data processor mutually exchanges data processing identifier information of other data processors ([McFarland et al.] Column 4 Lines 4-7 "Bus transactions between chips include the tag of the originating p-op").

Claim 9

The data processing circuit as claimed in claim 1 wherein the switch is provided with a queue temporarily holding data at a preceding stage of an input port or a subsequent stage of an output port ([McFarland et al.] Column 7 Lines 4-7 "P-ops that are not ready for immediate execution are stored in that unit's p-op queue").

Claim 10

A data processing circuit comprising: a processing destination identifier assigning portion which assigns, to data, processing destination identifiers indicating all data processing procedures determined by information included in the data ([McFarland et al.] Column 4 Line 11 "address preparation unit"); a switch which provides the data to a subsequent processing destination based on the processing destination identifiers

([McFarland et al.] Column 3 Line 48 "Instruction Decoder"), and a data processor which returns the data to the switch after performing predetermined processing to the data received from the switch ([McFarland et al.] Column 3 Line 34 "CPU").

Claim 11

The data processing circuit as claimed in claim 10 wherein the data processor deletes a processing destination identifier indicating its own processor ([McFarland et al.] Column 11 Line 26-29 "Backend termination bus logic 180 receives termination information from each of the functional units, making it possible for tracking logic 160 and abort logic 170 to maintain the status of each outstanding p-op").

Claim 12

The data processing circuit as claimed in claim 10 wherein the switch deletes a processing destination identifier of the subsequent processing destination ([McFarland et al.] Column 11 Line 20-21 "The Backend also includes abort logic 170 to handle aborting of p-ops").

Claim 13

The data processing circuit as claimed in claim 10 wherein the predetermined processing comprises traffic processing ([McFarland et al.] Column 1 Line 57-58 "parallel processing of instructions within and between functional units").

Claim 14

The data processing circuit as claimed in claim 10, further comprising a mother board which mounts the processing destination identifier assigning portion, the switch, and a connector which connects the switch and the data processor ([McFarland et al.] Column 4 Lines 1-2 "Each functional unit chip is packaged in a custom ceramic PGA which contains power and ground planes"), and a controller which manages a configuration state of the data processor and notifies the configuration state to the processing destination identifier assigning portion ([McFarland et al.] Column 4 Lines 1-2 "Each p-op issued by DEC 12 is given a tag which uniquely identifies each p-op currently outstanding in the machine" and Column 4 Lines 8-10 "DEC 12 is also responsible for tracking the status of outstanding p-op, pipeline control, and for invoking exception processing when needed").

Claim 15

The data processing circuit as claimed in claim 14, further comprising a memory which stores the configuration state of the data processor provided to the controller ([McFarland et al.] Column 4 Lines 51-53 "DTag 32 contains the address tag and line state bits for each line in DCache 35"). .

Claim 16

The data processing circuit as claimed in claim 15, further comprising an input portion inputting the configuration state to the memory ([McFarland et al.] Column 4

Lines 30-33 "A Memory and Cache Controller (MCC) 25 is responsible for controlling the instruction and data caches and implements the cache coherency protocol").

Claim 17

The data processing circuit as claimed in claim 14 wherein the data processor has data processing identifier information indicating its processing content, and the processing destination identifier assigning portion reads the data processing identifier information ([McFarland et al.] Column 4 Lines 1-2 "Each p-op issued by DEC 12 is given a tag which uniquely identifies each p-op currently outstanding in the machine" and Column 4 Lines 8-10 "DEC 12 is also responsible for tracking the status of outstanding p-op, pipeline control, and for invoking exception processing when needed").

Claim 18

The data processing circuit as claimed in claim 10 wherein the switch is provided with a queue temporarily holding data at a preceding stage of an input port or a subsequent stage of an output port ([McFarland et al.] Column 7 Lines 4-7 "P-ops that are not ready for immediate execution are stored in that unit's p-op queue").

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Farhad Ali whose telephone number is (571) 270-1920. The examiner can normally be reached on Monday thru Friday, 7:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey C. Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

F.A.

James K. Trujillo
James K. Trujillo
Primary Examiner
TC 2100